LTCC MATERIAL GUIDE

HiDEC utilizes the material Green Tape chemistries from DuPont or Ferro whether that be silver or gold. Information on product name and applications are shown below

TAPE PRODUCT	**DuPont 951**		**DuPont 9K7**		**Ferro L8**	
50.8µm thick Green sheet (2mil)	951C2				L8	
114.3µm thick Green sheet (4.5mil)	951PT					
127µm thick Green sheet (5mil)			9k7V		L8 (5.4mil)	
165.1µm thick Green sheet (6.5mil)	951P2				L8 (7.8mil)	
254µm thick Green sheet (10mil)	951PX		9K7X		L8 (12.1mil)	
APPLICATION CO-FIRE	**Ag**	**Au**	**Ag**	**Au**	**Ag**	**Au**
Via Fill	6141R	5738R	LL601	LL502	CN33-493	CN30-078PF
Transition Via Fill		6138R			CN39-005	
Internal Conductor	6142D	5742	LL612	LL505	CN33-498	CN30-030
Internal Ground Plane	6142D	5742	LL602	LL505	CN33-498	CN30-030
External Conductor	6142D	5742	LL612	LL507	CN33-498	CN30-030
External Ground Plane	6142D	5742	LL602	LL507	CN33-498	CN30-030
Wire Bondable (fine Au wire)		TC502		LL507		CN30-030
Wire Bondable (fine Al & Au wire)		5742				
Solderable	6146	5739	LL617	LL509	CN39-001	CN36-202
Plateable (NiAu)	6118A				CN33-495	
Overglaze	9651R	9651R				
APPLICATION POST-FIRE	**Ag**	**Au**	**Ag**	**Au**	**Ag**	**Au**
External Conductor	7484R	5771				
External Ground Plane	7484R	5771				
Wire Bondable (fine Au wire)		5771		LL507		3066-G
Wire Bondable (fine Al & Au wire)		5771				3068N
Solderable	7484R	4597	7484	4597	3309	CN31-014
Plateable (NiAu)	6119R					
Braze Adhesion Layer	5081R	5062D	5081R	5062D		
Braze Barrier Layer	5082R	5063D	5082R	5063D		
Braze Solder Alloy	5087	5087	5087	5087		4007-G
Overglaze	QQ550	QQ550				

LTCC PARAMETER GUIDELINES

The items provided here are the conventional parameters used to process LTCC.

LINE PARAMETER	**Conventional**	**Units/Description**
Line Width	150 (6)	Microns (mils)
Line to Line Spacing	150 (6)	Microns (mils)
Line to Substrate Edge Spacing	200 (8)	Microns (mils)
Line Thickness	12 (0.5)	Microns (mils)
VIA PARAMETER		
Via Diameter (127µm Tape)	150 (6)	Microns (mils)
Via Diameter (254µm Tape)	200 (8)	Microns (mils)
Via Capture Pad (beyond via diameter (D))	100 (4)	Microns (mils)
Via to Via Spacing	(1.5 * D) + D	
Via to Line Edge	150 (6)	Microns (mils)
Via to Substrate Edge	200 (8)	Microns (mils)
DESIGN GUIDELINE CONSIDERATIONS		
Tape Stacking	6 to 20	Layers
Maximum Fired Size	125 mm diameter or 100mm x 100mm	
Internal Power/Ground Plane Coverage	50% (as grid)	
Minimum Tape Stacking	6 layers or 1mm	
CAVITIES		
Cavity Width	2,500 (100)	Microns (mils)
Cavity Floor Thickness	500 (20)	Microns (mils)
Cavity Shelf Thickness	500 (20)	Microns (mils)
Cavity Shelf Width	1,000 (40)	Microns (mils)
Cavity Area vs. Surface Area	40%	

Design Considerations:

1. Consider using an overglaze for traces when soldering application required or any concerns with shorts.
2. Use similar layer to layer count (with equal metallization load) on both sides of substrate. This may require a dummy layer on the opposing side to minimize bowing of final product.

HIGH DENSITY ELECTRONIC CENTER
700 RESEARCH CENTER BLVD
FAYETTEVILLE, AR 72701

TELEPHONE: 479 575 2519
INFO@HIDEC.EDU
WWW.HIGH-DENSITY-ELECTRONICS.UARK.EDU